Summary	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
FetchMicrocode	80	106	50	56	50	56
ALU Binary -> Flags	198	321	60	98	50	81
1 Cycle BCD NMOS Flags	202	336	67	106	46	69
2 Cycle BCD CMOS Flags	125	213	42	67	26	43
ALU Binary No Flags	164	247	47	77	41	64
Increment DPH	200	312	59	96	50	78
BranchExit	189	327	64	101	47	73
1-Cycle NOP	143	276	59	97	47	75
Indexed Address Add	155	248	52	80	49	74
FetchOperand	153	238	47	75	44	69
FetchOpcode	153	238	47	75	44	69
Memory Read	190	193	52	66	46	54
Memory Write	190	274	52	86	46	74
6510 Port Read	194	302	54	94	43	72
6510 Port Write	162	270	50	86	41	70
Critical Path (2-Cycle BCD CMOS Flags)	200	327	64	101	50	81
Max Frequency (MHz)	**5.0**	3	**15.7**	10	**20.0**	12
Critical Path (1-Cycle BCD NMOS Flags)	202	336	67	106	50	81
Max Frequency (MHz)	**5.0**	3	**14.9**	9	**20.0**	12

Note: AC+ column includes TI 74CBT & 74LVC parts where noted. Midpoint between Min and Max tpd @ CL=15pF, 25˚, 5.0V used for "Typ" LVC parts.

Note: AC propagation times are from Fairchild Datasheets (50pf, 25˚C, 5.0V) unless otherwise noted.

Note: HC propagation times are from TI Datasheets (50pf, 25˚C, 4.5V) unless otherwise noted.

Note: Target clocks rates: 2-cycle BCD CMOS Flags 20MHz, 1-cycle BCD NMOS Flags 16.36MHz for NTSC

Component Inventory	Component	Desc	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
	7400	NAND	9.0	18.0	6.0	8.0	6.0	8.0
	7404	Inverter	9.0	19.0	4.0	7.0	4.0	7.0
	7408	AND	10.0	20.0	5.5	7.0	5.5	7.0
	7410	3-NAND	10.0	19.0	4.5	7.0	4.5	7.0
	7411	3-AND	10.0	20.0	4.0	8.0	4.0	8.0
	7427	3-NOR	10.0	18.0	4.1	7.9	4.1	7.9
	7432	OR	10.0	20.0	5.5	7.5	5.5	7.5
(Fairchild NC7SZ04 for AC+)	7404(1G)	Inverter	9.0	19.0	4.0	7.0	1.8	3.1
(Fairchild NC7SZ08 for AC+)	7408(1G)	AND	10.0	20.0	5.5	7.0	2.2	4.1
(TI 74LVC for AC+)	7410(1G)	3-NAND	10.0	19.0	4.5	7.0	1.7	2.7
(TI 74LVC for AC+)	7411(1G)	3-AND	10.0	20.0	4.0	8.0	2.1	3.1
	74138 AY	Decoder - A to Y	18.0	36.0	6.5	9.5	6.5	9.5
	74151 E	MUX - Enable to Y	15.0	25.0	6.5	10.0	6.5	10.0
	74151 S	MUX - Sel to Y	30.0	50.0	8.5	13.0	8.5	13.0
	74153 D	MUX - Data to Y	17.0	28.0	5.5	8.0	5.5	9.0
	74153 S	MUX - Sel to Y	21.0	30.0	6.5	11.0	6.5	11.0
	74161 CP	Counter	25.0	41.0	5.0	9.5	5.0	9.5
	74161 S	Counter	25.0	41.0	5.0	9.5	4.0	8.5
(Only TI parts available)	74238 AY	Decoder A to Y	17.0	30.0	8.8	13.6	8.8	13.6
	74245 E	Buffer Enable	23.0	46.0	5.5	9.0	5.5	9.0
(TI 74CBT3245 for AC+, CL = 50)	74245 T	Buffer TPD	15.0	21.0	3.5	6.5	0.25	0.25
(TI 74CBT3251 for AC+, CL =10)	74251 D	MUX - Data to Y	17.0	39.0	7.0	11.0	0.05	0.25
	74251 S	MUX - Sel to Y	21.0	41.0	8.5	13.0	8.5	13.0
(TI 74CBT3253 for AC+, CL = 10)	74253 D	MUX - Data to Y	17.0	28.0	5.5	8.0	0.05	0.3
(TI 74CBT3257 for AC+, CL=10)	74257 D	MUX - Data to Y	10.0	20.0	4.5	6.0	0.05	0.15
	74257 S	MUX - Sel to Y	10.0	20.0	4.5	6.0	4.5	6.0
(TI 74LVC for AC+)	7427(1G)	3-NOR	10.0	18.0	4.1	7.9	2.0	3.1
	74273 S	Register - Setup	10.0	20.0	2.5	4.0	2.5	4.0
	74273 T	Register - TPD	15.0	32.0	5.5	10.0	5.5	10.0
(TI for AC)	74283 CC	ADDR CIN - COUT	23.0	39.0	10.3	16.0	10.3	16.0
(TI for AC)	74283 CS	ADDR CIN - S	27.0	46.0	10.3	16.5	10.3	16.5
(TI for AC)	74283 DC	ADDR Data to COUT	23.0	39.0	10.6	16.5	10.6	16.5
(TI for AC)	74283 DS	ADDR Data to Sum	25.0	42.0	10.6	16.5	10.6	16.5
	74541 E	Buffer Enable	17.0	30.0	6.0	9.5	6.0	9.5
	74541 T	Buffer TPD	12.0	23.0	4.0	6.0	4.0	6.0
Enable with Collision (double)	74574 C	Register - Collision	41.6	60.0	12.0	19.0	12.0	19.0
	74574 E	Register - Enable	26.0	30.0	6.0	9.5	6.0	9.5
	74574 S	Register - Setup	10.0	20.0	0.0	1.5	0.0	1.5
	74574 T	Register - TPD	28.0	36.0	6.0	9.5	6.0	9.5
	74688 T	Comparator	22.0	35.0	22.0	35.0	22.0	35.0
	7474 S	Flip Flop Setup	10.0	20.0	1.0	3.0	1.0	3.0
	7474 T	Flip Flop TPD	20.0	35.0	5.9	10.0	6.0	10.0
(TI 74LVC for AC+)	7474(1G) S	Flip Flop Setup	10.0	20.0	1.0	3.0	1.1	1.1
(TI 74LVC for AC+)	7474(1G) T	Flip Flop TPD	20.0	35.0	5.9	10.0	3.0	4.4
	AT27C256R	ROM	45.0	45.0	45.0	45.0	45.0	45.0
	CY7C199CN	RAM	15.0	15.0	15.0	15.0	15.0	15.0

FLAGS

	Component	Desc	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
V Flag Evaluate	74151	S MUX - Sel to Y	30	50	8.5	13	8.5	13
V Select	74251	D MUX - Data to Y	17	39	7.0	11	0.05	0.25
			47	89	15.5	24	8.6	13
Z Flag Evaluate	7427	3-NOR	10	18	4.1	8	4.1	8
Z Flag Evaluate	7411	3-AND	10	20	4.0	8	4.0	8
Z Select	74251	D MUX - Data to Y	17	39	7.0	11	0.05	0.25
			37	77	15.1	27	8.2	16
C.OUT	74251	D MUX - Data to Y	17	39	7.0	11	0.05	0.25
C Select	74151	D Decoder - A to Y	18	36	6.5	10	6.5	10
			35	75	13.5	21	6.6	10
N Select	74151	D Decoder - A to Y	18	36	6.5	10	6.5	10
Max Flag			47	89	15.5	27	8.6	16

ALU Binary -> Flags

A := A ADC B; SETF(NZVC)	Component	Desc	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
MIR	74574	T Register - TPD	28	36	6.0	10	6.0	10
R.MX	74138	AY Decoder - A to Y	18	36	6.5	10	6.5	10
A.R OE	74574	E Register - Enable	26	30	6.0	10	6.0	10
LU	74153	S MUX - Sel to Y	21	30	6.5	11	6.5	11
ADDR L	74283	DC ADDR Data to COUT	23	39	10.6	17	10.6	17
SKIP.ADR	74257	S MUX - Sel to Y	10	20	4.5	6	4.5	6
LSR.OUT	74245	T Buffer TPD	15	21	3.5	7	0.25	0.25
Max Flag			47	89	15.5	27	8.6	16
P Register	7474	S Flip Flop Setup	10	20	1.0	3	1.0	3
			198	321	60	98	49.9	81

ALU BCD -> Flags

Note: BCD cycles follow FetchOperand (except decimal mode RRA and ISC). Preset R.MX=A means R.MX decoder is done in the pr

A := A ADC B	Component	Desc	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
B.R OE	74574	E Register - Enable	26	30	6.0	10	6.0	10
LU	74153	S MUX - Sel to Y	21	30	6.5	11	6.5	11
ADDR L	74283	DC ADDR Data to COUT	23	39	10.6	17	10.6	17
BCD.DETECT.LO	74151	S MUX - Sel to Y	30	50	8.5	13	8.5	13
BCD.SEL.LO	74257	D MUX - Data to Y	10	20	4.5	6	0.05	0.15
BCD.DETECT.HI	74251	D MUX - Data to Y	17	39	7.0	11	0.05	0.25
BCD.DETECT.HI.AUX	74253	D MUX - Data to Y	17.0	28.0	5.5	8.0	0.05	0.25
BCD.SEL.HI	74257	D MUX - Data to Y	10	20	4.5	6	0.05	0.15
BCD.ADJ.HI	74283	DC ADDR Data to COUT	23	39	10.6	17	10.6	17
BCD.OUT	74245	T Buffer TPD	15	21	3.5	7	0.25	0.25
Register Write	74574	S Register - Setup	10	20	0.0	2	0.00	2
Max Flag			47	89	15.5	27	8.6	16
P Register	7474	S Flip Flop Setup	10	20	1.0	3	1.0	3
2 Cycle BCD CMOS Flags			125	213	42	67	26.1	43
2 Cycle BCD NMOS Flags			101	168	34	53	22.8	35
1 Cycle BCD CMOS Flags			249	425	84	134	52.2	87
1 Cycle BCD NMOS Flags			202	336	67	106	45.7	69

ALU Binary No Flags

DPL := X + B	Component	Description	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
MIR	74574 E	Register - Enable	26	30	6.0	10	6.0	10
R.MX	74138 AY	Decoder - A to Y	18	36	6.5	10	6.5	10
DPH.R OE	74574 E	Register - Enable	26	30	6.0	10	6.0	10
LU	74153 S	MUX - Sel to Y	21	30	6.5	11	6.5	11
ADDR L	74283 DC	ADDR Data to COUT	23	39	10.6	17	10.6	17
SKIP.ADR	74257 S	MUX - Sel to Y	10	20	4.5	6	4.5	6
LSR.OUT	74245 T	Buffer TPD	15	21	3.5	7	0.25	0.25
W->DPH	74245 T	Buffer TPD	15	21	3.5	7	0.25	0.25
DPH Register	74574 S	Register - Setup	10	20	0.0	2	0.0	2
			164	247	47	77	40.6	64

Increment DPH

Note: MIR.SW switches to DPH := DPH + 1. Adds MIR.SW Enable time.

DPH := DPH + 1	Component	Description	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
MIR.SW FF	7474(1G) T	Flip Flop TPD	20	35	5.9	10	3.0	4
MIR - Enable w/ Collision	74574 C	Register - Collision	42	60	12.0	19	12.0	19
R.MX	74138 AY	Decoder - A to Y	18	36	6.5	10	6.5	10
DPH.R OE	74574 E	Register - Enable	26	30	6.0	10	6.0	10
LU	74153 S	MUX - Sel to Y	21	30	6.5	11	6.5	11
ADDR L	74283 DC	ADDR Data to COUT	23	39	10.6	17	10.6	17
SKIP.ADR	74257 S	MUX - Sel to Y	10	20	4.5	6	4.5	6
LSR.OUT	74245 T	Buffer TPD	15	21	3.5	7	0.25	0.25
W->DPH	74245 T	Buffer TPD	15	21	3.5	7	0.25	0.25
DPH Register	74574 S	Register - Setup	10	20	0.0	2	0.0	2
			200	312	59	96	49.6	78

BranchExit

PCL := PCL + B; EXIT.CC	Component	Description	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
MIR	74574 T	Register - TPD	28	36	6.0	10	6.0	10
R.MX	74138 AY	Decoder - A to Y	18	36	6.5	10	6.5	10
PCL.R OE	74574 E	Register - Enable	26	30	6.0	10	6.0	10
LU	74153 S	MUX - Sel to Y	21	30	6.5	11	6.5	11
ADDR L	74283 DC	ADDR Data to COUT	23	39	10.6	17	10.6	17
SKIP.ADR	74257 S	MUX - Sel to Y	10	20	4.5	6	4.5	6
C.OUT	74251 D	MUX - Data to Y	17	39	7.0	11	0.05	0.25
	7404	Inverter	9	19	4.0	7	4.00	7
BRANCH.EXIT	74251 D	MUX - Data to Y	17	39	7.0	11	0.05	0.25
	7410(1G)	3-NAND	10	19	4.5	7	1.7	3
MIR.SW FF	7474(1G) S	Flip Flop Setup	10	20	1.0	3	1.1	1
			189	327	64	101	47.0	73

1-Cycle NOP

STPWAI -> NOP1 -> FETCHOP	Component	Description	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
IR	74273 T	Register - TPD	15	32	5.5	10	5.5	10
CMOS1BOP	7404(1G)	Inverter	9	19	4.0	7	1.8	3
CMOS1BOP	7411(1G)	3-AND	10	20	4.0	8	2.1	3
CMOS1BOP	7432	OR	10	20	5.5	8	5.5	8
CMOS1BOP	7411(1G)	3-AND	10	20	4.0	8	2.1	3
CMOS1BOP	7408(1G)	AND	10	20	5.5	7	2.2	4
NOP1.DETECT	74151 E	MUX - Enable to Y	15	25	6.5	10	6.5	10
FETCHOP	7432	OR	10	20	5.5	8	5.5	8
NX.MX2	7432	OR	10	20	5.5	8	5.5	8
Q	7404	Inverter	9	19	4.0	7	4.0	7
Q	7411(1G)	3-AND	10	20	4.0	8	2.1	3
Q	74161 S	Counter	25	41	5.0	10	4.0	9
			143	276	59.0	97	46.7	75

Indexed Address Add

DPL := B + Y; INCDPH.C	Component	Description	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
MIR	74574 T	Register - TPD	28	36	6.0	10	6.0	10
R.MX	74138 AY	Decoder - A to Y	18	36	6.5	10	6.5	10
Y.R OE	74574 E	Register - Enable	26	30	6.0	10	6.0	10
LU	74153 S	MUX - Sel to Y	21	30	6.5	11	6.5	11
ADDR L	74283 DC	ADDR Data to COUT	23	39	10.6	17	10.6	17
SKIP.ADR	74257 S	MUX - Sel to Y	10	20	4.5	6	4.5	6
INC.DPH	7400	NAND	9	18	6.0	8	6.0	8
MIR.SW FF	7410(1G)	3-NAND	10	19	4.5	7	1.7	3
MIR.SW FF	7474(1G) S	Flip Flop Setup	10	20	1.0	3	1.1	1
			155	248	52	80	48.9	74

FetchOperand

B := DPL := *PC; PC += 1	Component	Desc	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
MIR	74574 E	Register - Enable	26	30	6.0	10	6.0	9.5
AD.MX	74138 AY	Decoder - A to Y	18	36	6.5	10	6.5	10
PCH.ADL OE	74574 E	Register - Enable	26	30	6.0	10	6.0	10
INC2 ADDR	74283 CC	ADDR CIN - COUT	23	39	10.3	16	10.3	16
INC3 ADDR	74283 DS	ADDR Data to Sum	25	42	10.6	17	10.6	17
SKIP.ADR	74257 S	MUX - Sel to Y	10	20	4.5	6	4.5	6
S->PCH	74245 T	Buffer TPD	15	21	3.5	7	0.25	0.25
PCH Register	74574 S	Register - Setup	10	20	0.0	2	0.00	2
			153	238	47	75	44.1	69

FetchOpcode

Note: MIR.SW may switch for a FetchOpcode for Branch.Exit or NOP1. If so, AD.MX pre-set to *PC already. No collision or de

IR := *PC; PC += 1	Component	Desc	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
MIR	74574 E	Register - Enable	26	30	6.0	10	6.0	9.5
AD.MX	74138 AY	Decoder - A to Y	18	36	6.5	10	6.5	10
PCH.ADL OE	74574 E	Register - Enable	26	30	6.0	10	6.0	10
INC2 ADDR	74283 CC	ADDR CIN - COUT	23	39	10.3	16	10.3	16
INC3 ADDR	74283 DS	ADDR Data to Sum	25	42	10.6	17	10.6	17
SKIP.ADR	74257 S	MUX - Sel to Y	10	20	4.5	6	4.5	6
S->PCH	74245 T	Buffer TPD	15	21	3.5	7	0.25	0.25
PCH Register	74574 S	Register - Setup	10	20	0.0	2	0.00	2
			153	238	47	75	44.1	69

Memory Read

If Swithing back from DPH := DPH + 1, then AD.MX already preset - no collision or decoder delay, so not on the critical pa

A := MEM R	Component	Description	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
MIR	74574 E	Register - Enable	26	30	6.0	10	6.0	10
AD.MX	74138 AY	Decoder - A to Y	18	36	6.5	10	6.5	10
DPL.AD	7411	3-AND	10	20	4.0	8	4.0	8
DPL.AD OE	74574 E	Register - Enable	26	30	6.0	10	6.0	10
ADL.A	74245 T	Buffer TPD	15	21	3.5	7	0.3	0
RAM	CY7C199CN	RAM	15	15	15.0	15	15.0	15
ALU.BYPASS	74245 T	Buffer TPD	15	21	3.5	7	0.25	0.25
A Register	74574 S	Register - Setup	10	20	0.0	2	0.0	2
			135	193	44.5	66	38.0	54

Memory Write

If Swithing back from DPH := DPH + 1, then AD.MX already preset - no collision or decoder delay, so not on the critical pa

*DP := X	Component	Description	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
MIR	74574 E	Register - Enable	26	30	6.0	10	6.0	10
AD.MX	74138 AY	Decoder - A to Y	18	36	6.5	10	6.5	10
DPL.AD	7411	3-AND	10	20	4.0	8	4.0	8
DPL.AD OE	74574 E	Register - Enable	26	30	6.0	10	6.0	10
ADL.A	74245 T	Buffer TPD	15	21	3.5	7	0.3	0
Must be ok at half-cycle			95	137	26.0	43	22.8	37
Symetrical Full Cycle			190	274	52.0	86	45.5	74

6510 Port Read

If Swithing back from DPH := DPH + 1, then AD.MX already preset - no collision or decoder delay, so not on the critical pa

A := MEM R (6510)	Component	Description	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
MIR	74574 E	Register - Enable	26	30	6.0	10	6.0	10
AD.MX	74138 AY	Decoder - A to Y	18	36	6.5	10	6.5	10
DPL.AD	7411	3-AND	10	20	4.0	8	4.0	8
DPL.AD OE	74574 E	Register - Enable	26	30	6.0	10	6.0	10
ADL.A	74245 T	Buffer TPD	15	21	3.5	7	0.3	0
PB.CS	7427	3-NOR	10	18	4.1	8	4.1	8
PB.CS	7411(1G)	3-AND	10	20	4.0	8	2.1	3
PB.CS	7411(1G)	3-AND	10	20	4.0	8	2.1	3
PBDA	74138 AY	Decoder - A to Y	18	36	6.5	10	5.5	10
PDR -> D	74574 E	Register - Enable	26	30	6.0	10	6.0	9.50
ALU.BYPASS	74245 T	Buffer TPD	15	21	3.5	7	0.25	0.25
A Register	74574 S	Register - Setup	10	20	0.0	2	0.0	2
			194	302	54.1	94	42.7	72

6510 Port Write

If Swithing back from DPH := DPH + 1, then AD.MX already preset - no collision or decoder delay, so not on the critical pa

A := MEM R (6510)	Component	Description	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
MIR	74574 E	Register - Enable	26	30	6.0	10	6.0	10
AD.MX	74138 AY	Decoder - A to Y	18	36	6.5	10	6.5	10
DPL.AD	7411	3-AND	10	20	4.0	8	4.0	8
DPL.AD OE	74574 E	Register - Enable	26	30	6.0	10	6.0	10
ADL.A	74245 T	Buffer TPD	15	21	3.5	7	0.3	0
PB.CS	7427	3-NOR	10	18	4.1	8	4.1	8
PB.CS	7411(1G)	3-AND	10	20	4.0	8	2.1	3
PB.CS	7411(1G)	3-AND	10	20	4.0	8	2.1	3
PBAD	74138 AY	Decoder - A to Y	18	36	6.5	10	5.5	10
6510 WR Latch	7404	Inverter	9	19	4.0	7	4.0	7
6510 WR Latch	7474 S	Flip Flop Setup	10	20	1.0	3	1.0	3
			162	270	49.6	86	41.5	70

FetchMicrocode

MIR := ROM[Q]	Component	Description	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
Q.REG	74161 CP	Counter	25	41	5.0	10	5.0	10
ROM	AT27C256R	ROM	45	45	45.0	45	45.0	45
MIR	74574 S	Register - Setup	10	20	0.0	2	0.0	2
			80	106	50.0	56	50.0	56

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